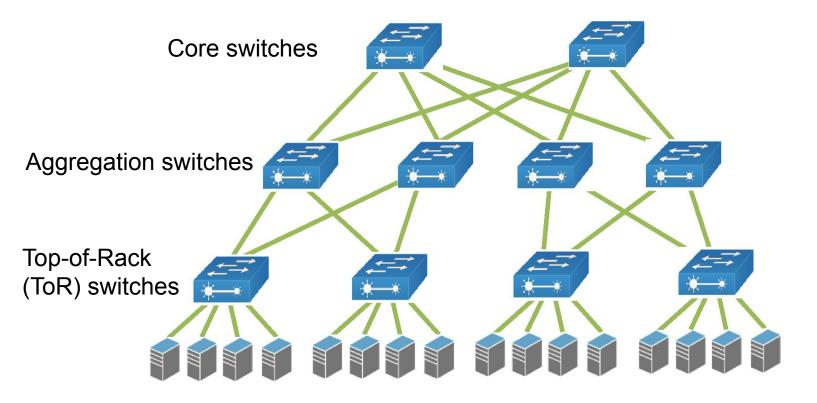
Hop-On Hop-Off Routing

A Fast Tour across the Optical Data Center Network for Latency-Sensitive Flows

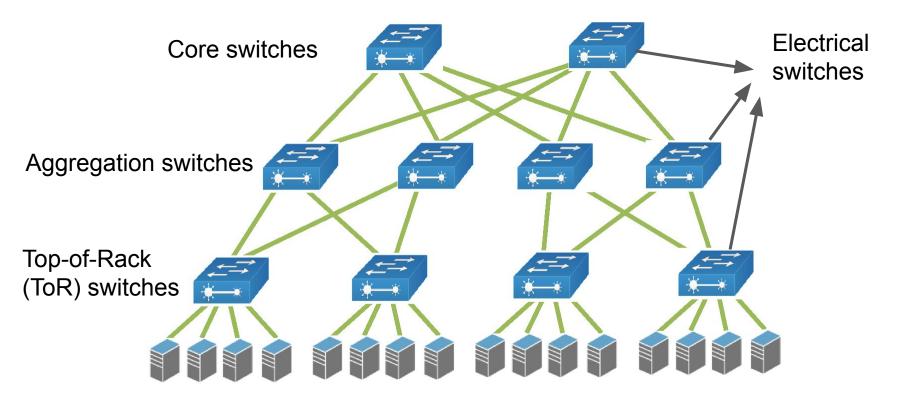
Jialong Li¹, Yiming Lei¹, Federico de Marchi² Raj Joshi³, Balakrishnan Chandrasekaran⁴, Yiting Xia¹

Max Planck Institute for Informatics
 Saarland University
 National University of Singapore
 Vrije Universiteit Amsterdam

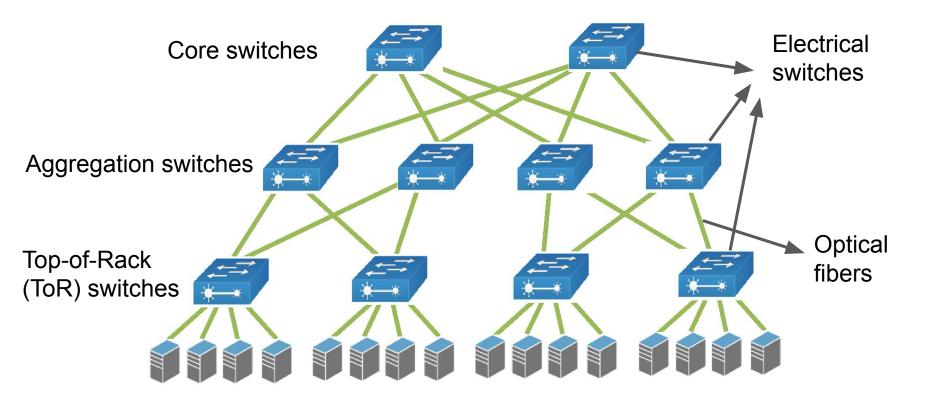
Today's Data Center Networks



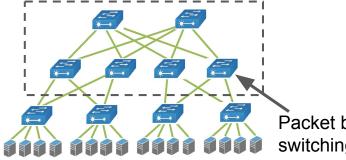
Today's Data Center Networks



Today's Data Center Networks



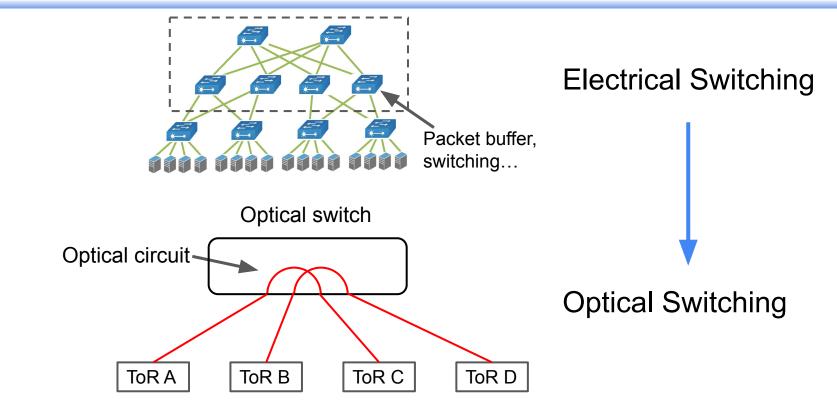
From Electrical Switching to Optical Switching



Electrical Switching

Packet buffer, switching...

From Electrical Switching to Optical Switching



Why Optical Switching

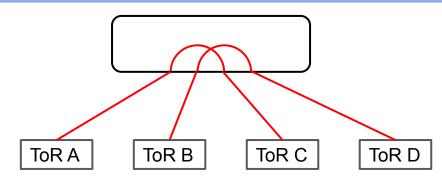
- No queuing delay along the circuit

Why Optical Switching

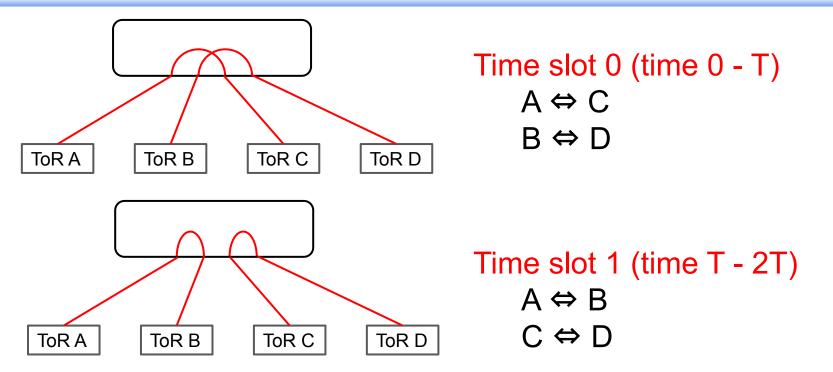
- No queuing delay along the circuit
- Less power consumption

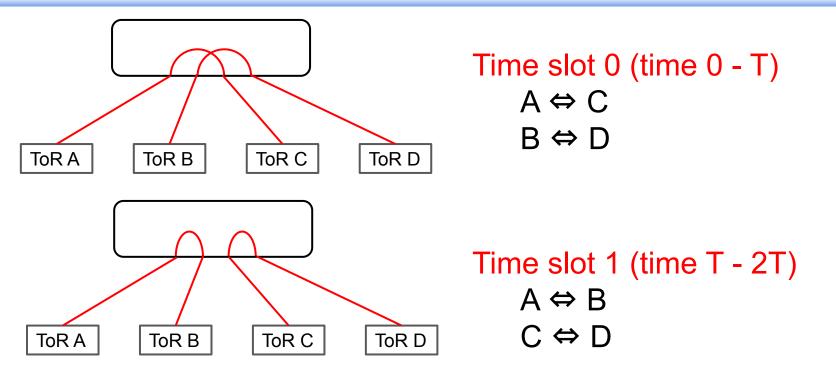
Why Optical Switching

- No queuing delay along the circuit
- Less power consumption
- Independent to link bandwidth

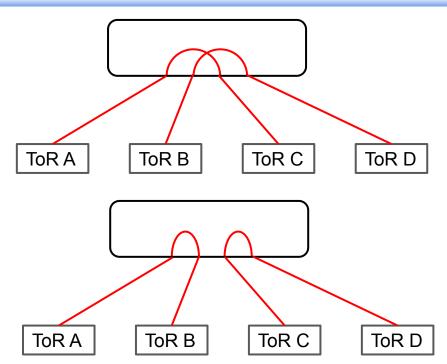


Time slot 0 (time 0 - T) $A \Leftrightarrow C$ $B \Leftrightarrow D$

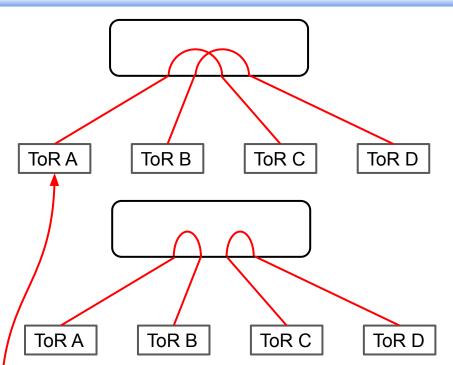




Time slot: When and how long the circuit exists



- A packet arrives at time 0
- Src = A, dst = B
- Waiting at A for time T



- A packet arrives at time 0
- Src = A, dst = B
- Waiting at A for time T

Circuit waiting delay: delay at src ToR before required circuit comes

Latency-Sensitive Flows: Flow Completion Time (FCT) is critical

Latency-Sensitive Flows: Flow Completion Time (FCT) is critical

FCT: tens of *ns* to hundreds of $\mu s^{[1]}$ Circuit waiting delay: tens of μs to *ms* Latency-Sensitive Flows: Flow Completion Time (FCT) is critical

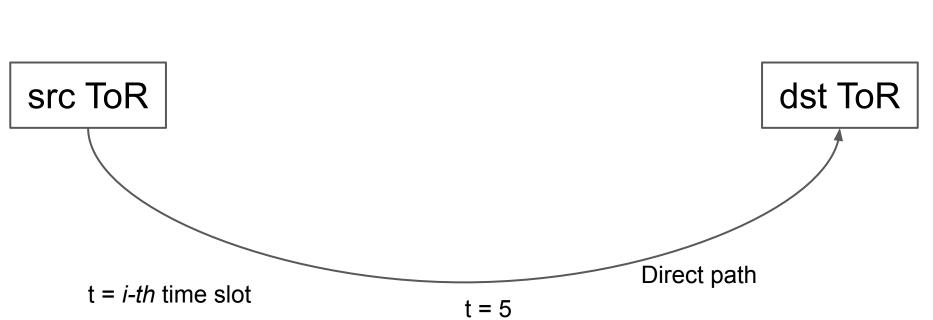
FCT: tens of *ns* to hundreds of $\mu s^{[1]}$

Circuit waiting delay: tens of μs to ms

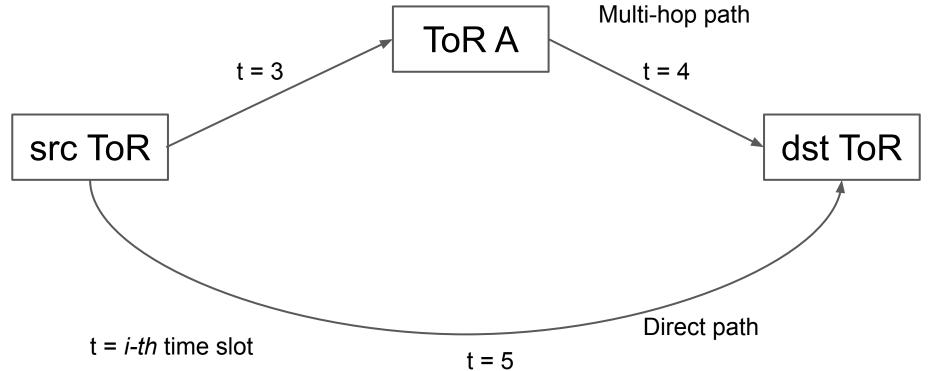
Reduce circuit waiting delay: Using multi-hop paths

[1] Expanding across time to deliver bandwidth efficiency and low latency, NSDI' 20

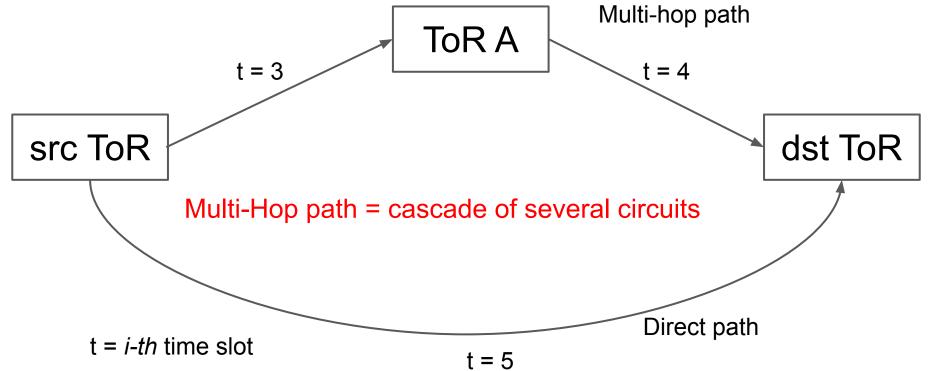
Multi-Hop Path



Multi-Hop Path



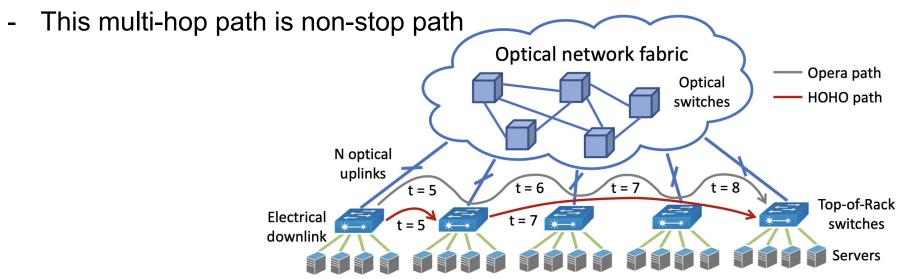
Multi-Hop Path



State-of-the-art: Opera (NSDI' 2020)

Opera

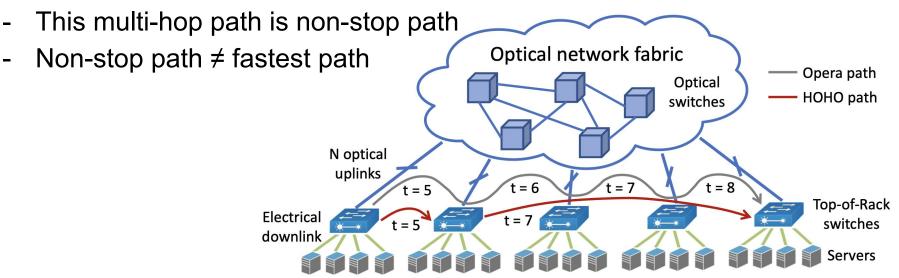
 A multi-hop path is available at any moment between any ToR pairs



State-of-the-art: Opera (NSDI' 2020)

Opera

 A multi-hop path is available at any moment between any ToR pairs



Hop-On Hop-Off (HOHO) Routing

- Search for the fastest path, instead of non-stop paths
- Packets could wait at ToRs, so they can "hop on" a circuit, "hop off", and "hop on" another circuit

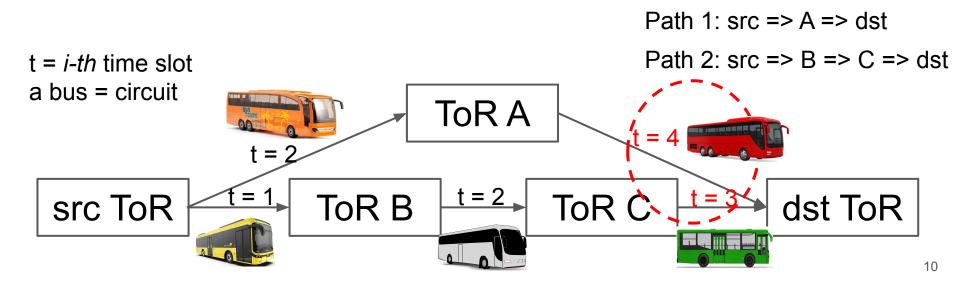


HOHO Routing: Intuition

- The latency of a path is only determined by the time slot of the last-intermediate ToR and dst ToR

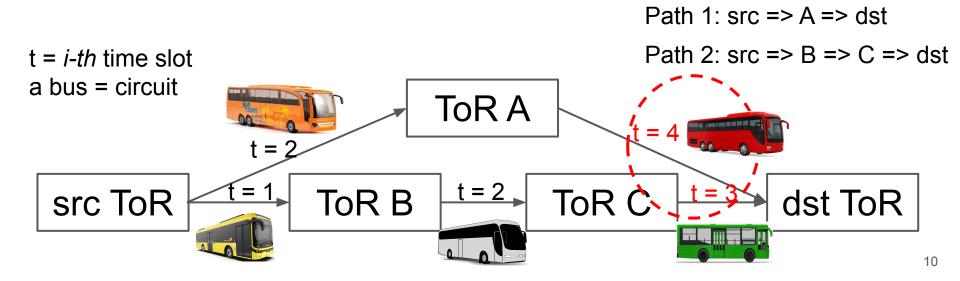
HOHO Routing: Intuition

- The latency of a path is only determined by the time slot of the last-intermediate ToR and dst ToR



HOHO Routing: Intuition

- The latency of a path is only determined by the time slot of the last-intermediate ToR and dst ToR
- Backtracking: Search from dst ToR to src ToR



Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D

Fixed, periodic optical schedule

- Time slot index indicating when two ToRs have a circuit

Input

- A fixed, periodic optical schedule
- Src and dst ToR
- Packet arrival time slot
- Maximum hops (optional)

Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D

Fixed, periodic optical schedule

- Time slot index indicating when two ToRs have a circuit

Input

- A fixed, periodic optical schedule
- Src and dst ToR
- Packet arrival time slot
- Maximum hops (optional)

Output

- A fastest path between src and dst ToR

Rerun per ToR pair, per packet arrival time slot

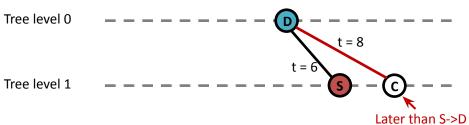
Send a packet from S to D in the minimal time within max hops, max = 3 here

Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D

Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



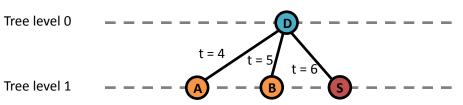
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



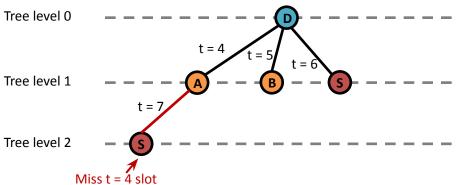
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



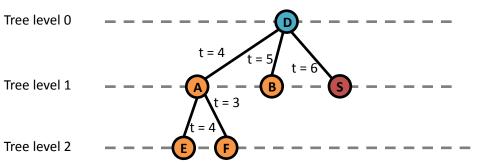
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



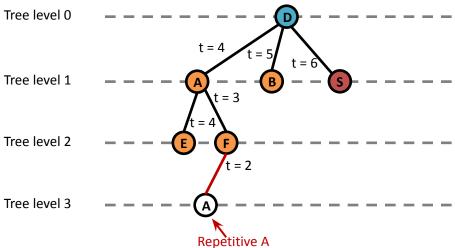
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



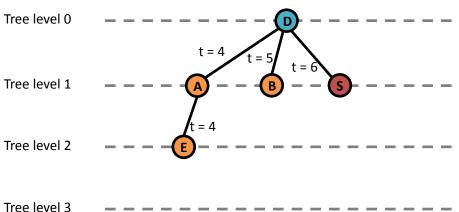
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



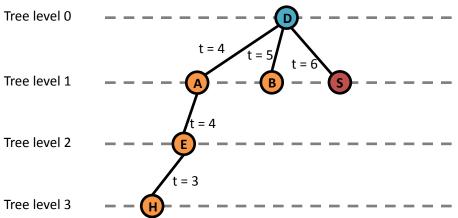
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



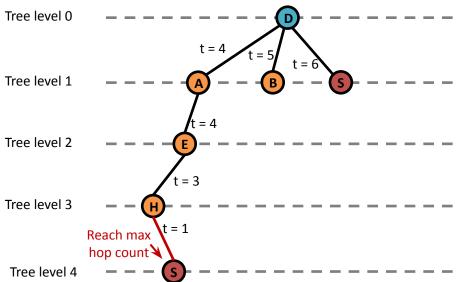
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



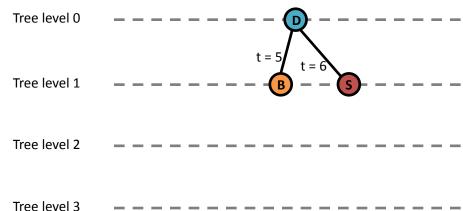
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



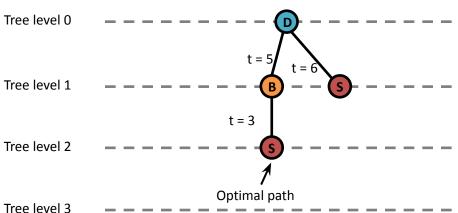
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



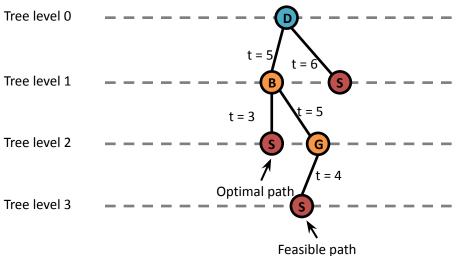
Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



Time Slot	Circuits
1	S – H
2	A – F
3	H – E, F – A, S – B
4	S – G, A – D
5	B – D, G – B
6	S – D
7	S – A
8	C – D



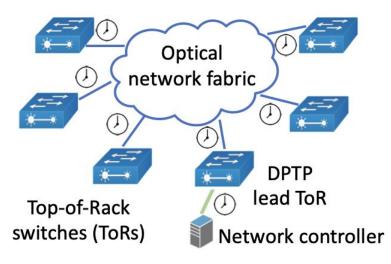
HOHO Routing: Features

- Backtracking
 - Search from dst to src ToR
- Optimal
 - Generate the fastest and shortest path
- Offline
 - Calculate offline and build routing table
- Decouple algorithm and run-time system designs
 - Assume no queuing delay at offline calculation and consider this at run-time system

System Design: Time Synchronization

- Every ToR needs to know when to send packet
- Leverage existing protocols
 - DPTP^[1], nanosecond-level synchronization precision

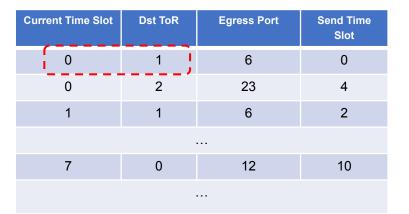
Time synchronization

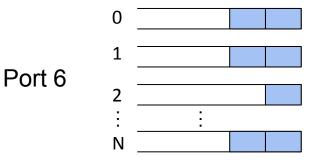


- HOHO generates a routing table
 - Current time slot: when the packet arrives
 - Dst ToR: final destination ToR
 - Egress port
 - Send time slot: when to send out
 - the packet

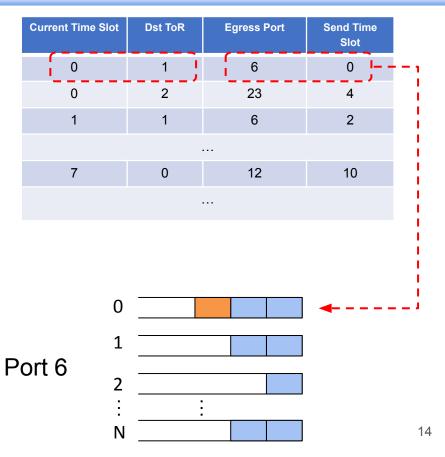
Current Time Slot	Dst ToR	Egress Port	Send Time Slot
0	1	6	0
0	2	23	4
1	1	6	2
7	0	12	10

- Look up current time slot and dst
 ToR to get egress port and send time slot
 - Packet with current time slot 0 and dst ToR 1



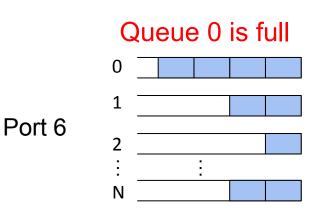


- Look up current time slot and dst
 ToR to get egress port and send time slot
 - Packet with current time slot 0 and dst ToR 1
 - Buffer at queue 0



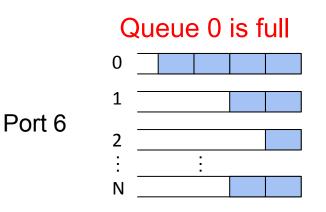
 If missing the planned send time slot due to the queue occupancy, look up from next current time slot

Current Time Slot	Dst ToR	Egress Port	Send Time Slot
0	1	6	0
0	2	23	4
1	1	6	2
7	0	12	10

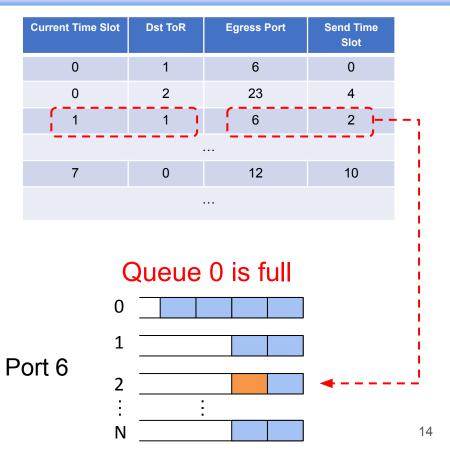


- If missing the planned send time slot due to the queue occupancy, look up from next current time slot
 - Move to current time slot 1

Current Time Slot	Dst ToR	Egress Port	Send Time Slot
0	1	6	0
0	2	23	4
1	1	6	2
7	0	12	10

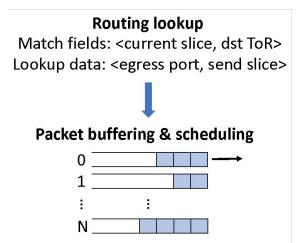


- If missing the planned send time slot due to the queue occupancy, look up from next current time slot
 - Move to current time slot 1
 - Buffer at queue 2



System Design: Buffering

- Packet is buffered at the queue before its sending time slot
- Could be realized by queue pause



Setup

- Reused the setup in Opera paper^[1]
 - Topology: 108 ToRs and 648

servers, each ToR with six 10G

downlinks to servers and six 10G

uplinks to optical fabric

- Workload: 1%~40% data-mining

traffic from Microsoft

[1] Expanding across time to deliver bandwidth efficiency and low latency, NSDI' 20

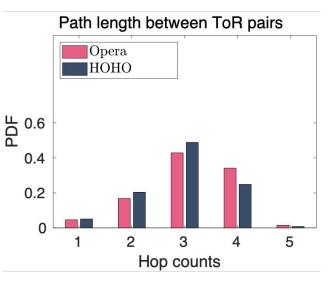
Setup

- Reused the setup in Opera paper^[1]
- Topology: 108 ToRs and 648 servers, each ToR with six 10G downlinks to servers and six 10G uplinks to optical fabric
- Workload: 1%~40% data-mining

traffic from Microsoft

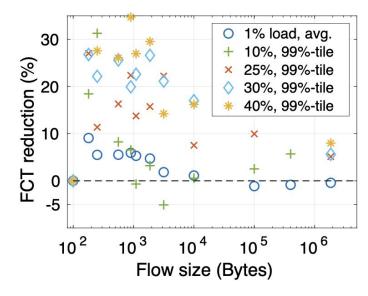
[1] Expanding across time to deliver bandwidth efficiency and low latency, NSDI' 20

Shorter paths



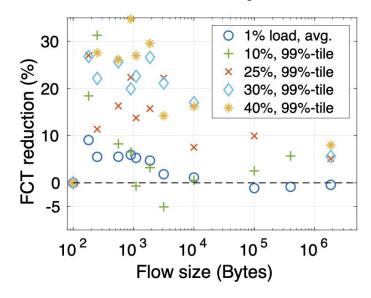
- Avg. hops: 3.11 => 2.80
- >= 4 hops: 37% => <mark>25%</mark>

Lower latency

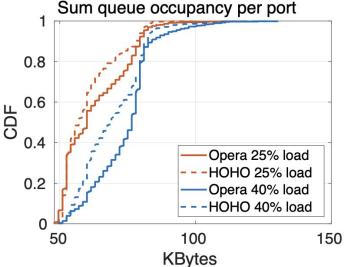


- FCT reduction: up to 35%

Lower latency



Lower queue occupancy



- FCT reduction: up to 35%

Queue occupancy reduction: 5%
 (25% load) and 10% (40% load)

Summary

- Hop-On Hop-Off optical circuits
 - Allow packets to "wait" at ToRs
- HOHO routing algorithm
 - Works on any optical schedule
 - Optimal (fastest and shortest path)
- A system sketch
 - Time synchronization + routing lookup + buffer management
- Simulation
 - Shorter paths, lower FCT, lower queue occupancy

